

### **REMARKS**

Claims 1-21 are now pending in the present application. Claims 1-10 and 20 stand rejected pursuant to an Office Action dated 9/23/2005. Claims 11-19 have previously been withdrawn from consideration. Claims 1 and 20 have been amended, and Claim 21 has been added, herewith. Reconsideration of the claims is respectfully requested.

#### **I. 35 U.S.C. § 112, Second Paragraph**

The Examiner rejected Claim 20 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter, which applicants regard as the invention. This rejection is respectfully traversed.

The Examiner states in rejecting Claim 20 that "It is not clear how the resistor of claim 1 can be in a circuit without a voltage at each terminal. This is a bias voltage, since there is a voltage". Applicants traverse as follows.

'Bias voltage' does not mean the same thing as 'voltage'. If they did, there would be no reason for the word 'bias', as it would provide no additional meaning over and above what is meant by the word 'voltage'. This is obviously not the case, and bias voltage does not mean the same thing as voltage as those terms are known to those of ordinary skill in the art. A bias voltage is commonly known to be a DC voltage used to bias a circuit to place the circuit in a particular steady state condition such that it can then process waveforms/signals of varying voltages that may also appear in the circuit. For example, an amplifier is typically biased to place the circuit in its proper operating state to amplify a signal, and then a voltage signal (which is not a bias voltage) may be applied to the input of the amplifier to provide amplification of such applied signal at the output of the amplifier. Attachments 1 and 2 attached hereto further evidence that a bias voltage is commonly known to those of ordinary skill in the art as a DC voltage used to place a circuit in a given steady state, and this term does not merely mean a 'voltage'. In any event, Applicants have amended Claim 20 to overcome such un-common interpretation of the term 'bias voltage'.

Therefore the rejection of Claim 20 under 35 U.S.C. § 112, second paragraph has been overcome.

## II. 35 U.S.C. § 102, Anticipation

The Examiner rejected Claims 1, 3 and 5-6 under 35 U.S.C. § 102(b) as being anticipated by Dorda et al. (4,219,829). This rejection is respectfully traversed.

With respect to Claim 1, it is urged that the cited reference does not teach a diffusion resistor, but instead teaches a transistor – specifically a field effect transistor. This can be seen by Dorda's description of the Figures, where it states at col. 4, lines 1-14:

FIG. 1 is a schematic representation, in cross section, of a **field effect transistor** constructed in accordance with the invention;

FIG. 2 is a schematic representation, in cross section, of a **field effect transistor** constructed in accordance with the invention;

FIG. 3 is a schematic representation, in cross section, of a **field effect transistor** constructed in accordance with the invention and having a Schottky gate electrode; and

FIG. 4 is a schematic circuit diagram of an oscillator constructed with a **field effect transistor**, according to the present invention, wherein the field effect transistor has been replaced by its equivalent circuit diagram.

These are the only figures in the Dorda patent, and thus it is urged that *every embodiment of Dorda describes a field-effect transistor*, and not a diffusion resistor as claimed. For a prior art reference to anticipate in terms of 35 U.S.C. 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

This difference can also be seen by Dorda's description at col. 4, lines 53-55 where a bias voltage is required to be provided on the drain electrode 5 for proper operation of the field effect transistor (and without such bias voltage, the device provides no functionality at all). Claim 1 expressly recites "wherein the first conductive contact and the second conductive contact form two ends of the diffusion resistor with no bias voltage on either of the first conductive contact and the second conductive contact. Thus, it is further shown that Claim 1 is not anticipated by the cited reference.

Applicants traverse the rejection of Claims 3 and 5-6 for similar reasons to those given above with respect to Claim 1 (of which Claim 3 depends upon).

Therefore, the rejection of Claims 1, 3 and 5-6 under 35 U.S.C. § 102(b) has been overcome.

### **III. 35 U.S.C. § 102, Anticipation**

The Examiner rejected Claims 1 and 4 under 35 U.S.C. § 102(b) as being anticipated by Nelson (3,566,219). This rejection is respectfully traversed.

Applicants have amended Claim 1 to recite that the third contact that is connected to the surface of the substrate is *electrically isolated from the first conductive contact and the second conductive contact*. In contrast, Nelson teaches two contacts 46 and 47, with no separate third contact which is electrically isolated from the first conductive contact and the second conductive contact, as claimed. Thus, the amendment to Claim 1 has overcome the present rejection.

Applicants further urge that Claim 1 is not obvious in view of the cited reference. Although a device may be capable of being modified to run the way [the patent applicant's] apparatus is claimed, there must be a suggestion or motivation *in the reference* to do so. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Nelson requires a common connection between N+ region 38 and P region 34 for proper device operation (col. 2, lines 58-61). Thus, there would have been no motivation per the teachings of this reference to modify such teachings in accordance with amended Claim 1.

Applicants traverse the rejection of Claim 4 for similar reasons to those given above with respect to Claim 1 (of which Claim 4 depends upon).

Therefore, the rejection of Claims 1 and 4 under 35 U.S.C. § 102(b) has been overcome.

### **IV. 35 U.S.C. § 102, Anticipation**

The Examiner has rejected Claim 1 under 35 U.S.C. § 102(b) as being anticipated by Gray (6,087,193). This rejection is respectfully traversed.

The diffusion resistor of the present invention is substantially different from the regulated field emitter device as taught by the cited Gray reference. As shown by Gray's Figures 24 and 26, both the source and extractor gate require particular bias voltages for proper operation of the field emitter device, and thus this device cannot be used as diffusion resistor due to such biasing.

For example, as shown in Grey's Figure 24 and 26, and extractor-gate to source bias voltage  $V_1$  is required. Claim 1 expressly recites (1) "wherein the first conductive contact and the second conductive contact form two ends of the diffusion resistor with no bias voltage on either of the first conductive contact and the second conductive contact" and (2) "wherein the third contact forms a Schottky diode with a voltage being applied to the third contact to form a depletion region that changes in size depending on the voltage applied to the third contact to change a resistance in the diffusion resistor". The cited reference does not teach or otherwise suggest such a diffusion resistor having two non-biased ends and a voltage applied to a third contact between these two non-biased ends to form a depletion region, and thus it is urged that amended Claim 1 is not anticipated by the cited Gray reference.

In addition, the drain of Gray's field emitter device is not in electrical contact with any external component as its purpose is to provide a contact-less source of electrons (col. 4, lines 6-14; col. 4 line 66 – col. 5, line 10; col. 1, lines 23-29). Thus, there is no teaching of the claimed feature that the first conductive contact and the second conductive contact form two ends of the diffusion resistor, as the FET drain is explicitly required to not be in any type of external electrical contact and thus could not function to be a terminal of a diffusion resistor. Because the extractor gate 170 and collector anode 160 are used for controlling operation of the field emitter device itself (by the proper application of bias voltages), they too could not function to be a terminal of a diffusion resistor. As every element of the claimed invention is not identically shown in a single reference, it is urged that amended Claim 1 is not anticipated by the cited reference.

Therefore, the rejection of Claim 1 under 35 U.S.C. § 102(b) has been overcome.

#### V. 35 U.S.C. § 103, Obviousness

The Examiner rejected Claim 1 under 35 U.S.C. § 103(a) as being unpatentable over Gray (6,087,193) in view of Hayama (5,260,595). This rejection is respectfully traversed.

The fact that a prior art device could be modified so as to produce the claimed device is not a basis for an obviousness rejection *unless the prior art suggested the desirability of such a modification*. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). The cited references do not suggest any desire to modify such teachings in accordance with the features recited in Claim 1. For example, Gray *requires bias voltages to be applied to both the source*

and extractor gate for proper operation of the field emitter device, and thus this device cannot be used as a diffusion resistor due to such biasing. Thus, it is shown that there was no teaching, suggestion or other motivation to modify the teachings of the cited references in accordance with the particulars of the claimed diffusion resistor recited in Claim 1.

Therefore, the rejection of Claim 1 under 35 U.S.C. § 103(a) has been overcome.

**VI. 35 U.S.C. § 103, Obviousness**

The Examiner rejected Claims 3 and 5-7 under 35 U.S.C. § 103(a) as being unpatentable over Gray (6,087,193) (with Hayama above as necessary) or Nelson (3,566,219), in view of Bhatia et al. (4,426,655). This rejection is respectfully traversed.

Applicants traverse such rejection for similar reasons to those given above with respect to Claim 1 and the missing claimed features identified with respect to the cited Gray and Nelson references, and the improper modification of Gray in view of Hayama.

Therefore, the rejection of Claims 3 and 5-7 under 35 U.S.C. § 103(a) has been overcome.

**VII. 35 U.S.C. § 103, Obviousness**

The Examiner rejected Claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Gray (6,087,193) (with Hayama above as necessary), or Nelson (3,566,219), or Dorda et al. (4,219,829), in view of Kluth (6,521,515). This rejection is respectfully traversed.

Applicants traverse such rejection for similar reasons to those given above with respect to Claim 1 and the missing claimed features identified with respect to the cited Gray, Nelson and Dorda references, and the improper modification of Gray in view of Hayama.

Therefore, the rejection of Claim 2 under 35 U.S.C. § 103(a) has been overcome.

**VIII. 35 U.S.C. § 103, Obviousness**

The Examiner rejected Claim 4 under 35 U.S.C. § 103(a) as being unpatentable over Gray (6,087,193) (with Hayama above as necessary), or Dorda et al. (4,219,829), in view of Racanelli et al. (5,532,175). This rejection is respectfully traversed.

Applicants traverse such rejection for similar reasons to those given above with respect to Claim 1 and the missing claimed features identified with respect to the cited Gray and Dorda references, and the improper modification of Gray in view of Hayama.

Therefore, the rejection of Claim 4 under 35 U.S.C. § 103(a) has been overcome.

**IX. 35 U.S.C. § 103, Obviousness**

The Examiner rejected Claims 8-9 under 35 U.S.C. § 103(a) as being unpatentable over Gray (6,087,193) (with Hayama above as necessary), Nelson (3,566,219), or Dorda et al. (4,219,829), in view of Yu (2004/0075146). This rejection is respectfully traversed.

Applicants traverse such rejection for similar reasons to those given above with respect to Claim 1 and the missing claimed features identified with respect to the cited Gray, Nelson and Dorda references, and the improper modification of Gray in view of Hayama.

Therefore, the rejection of Claims 8-9 under 35 U.S.C. § 103(a) has been overcome.

**X. 35 U.S.C. § 103, Obviousness**

The Examiner rejected Claim 20 under 35 U.S.C. § 103(a) as being unpatentable over Dorda et al. (4,219,829), in view of Gerlach (3,320,550). This rejection is respectfully traversed.

Applicants initially traverse such rejection for similar reasons to those given above with respect to amended Claim 1 and the missing claimed features identified with respect to the cited Dorda reference.

Further, while the cited Gerlach reference describes use of negative-resistance diodes in the narrow sidewalls of a rectangular waveguide (col. 3, lines 18-21), these negative resistance diodes also require a separate bias voltage for proper operation (col. 3, lines 23-25; col. 4, lines 27-32). Thus, these teachings exhibit the same deficiency as the cited Dorda reference, in requiring a special bias voltage at the diode terminals for proper operation. Still further, there would have been no motivation to modify the teachings of Gerlach in accordance with the present invention recited in Claim 20, as Gerlach requires that these diodes be biased in order that these diodes can provide proper amplification that is required for the waveguide wall-current tunnel diode amplifier and oscillator (col. 4, lines 32-36). This diode biasing for amplification purposes also evidences that these tunnel diodes are not resistors as that term is commonly known to those of ordinary skill in the art. Therefore, the cited Gerlach does not teach or

otherwise suggest the missing claimed features of Claim 20 that are not taught by the cited Dorda reference, and thus it is urged that Claim 20 is not obvious in view of the cited references.

Therefore, the rejection of Claim 20 under 35 U.S.C. § 103(a) has been overcome.

**XI. Newly Added Claim 21**

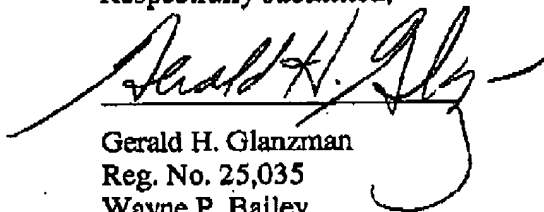
Claim 21 has been added herewith. Examination of such claim is respectfully requested.

**XII. Conclusion**

It is respectfully urged that the subject application is patentable over the cited references and is now in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: December 20, 2005

Respectfully submitted,



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IMI Technical Information

Attachment

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**Calibration**

Selecting &amp; Installing Accelerometers

**Troubleshooting Using Bias Voltage**

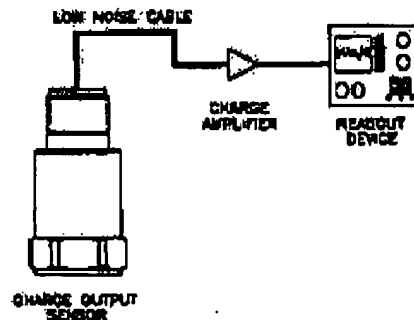
Mounting Techniques

Powering ICP® Accelerometers

Driving Long Cable Lengths

**Troubleshooting Using Bias Voltage****Using Bias Voltage as a Diagnostic Tool**

Piezoelectric sensors are dynamic measuring equip. They use piezoelectric sensing elements to convert (transduce) the mechanical phenomena to an electric signal. The mechanical parameter may be force, pressure or vibration. The raw electrical signal from a piezoelectric element is a high impedance charge signal. This charge signal is normally converted to a low impedance voltage signal by either an external charge amplifier or an external voltage amplifier. The cables between the charge sensor and the amplifier must be high quality, low noise cables must be kept as short as possible.



Internally amplified sensors, or ICP® sensors, employ miniature amplifiers to convert the high impedance charge signal into a low impedance voltage signal. These are internal to the sensor and therefore do not require noise cables or external amplifiers. These amplifiers are set gain so that output sensitivities are standardized.

<http://www.imi-sensors.com/technical/trouble.asp>

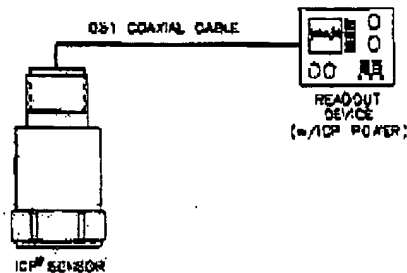
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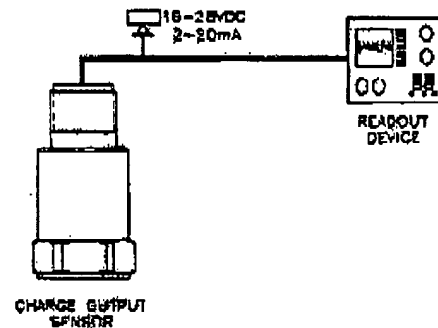
IMI Technical Information

Attachment 1

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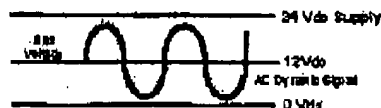
ICP® sensors are two wire sensors. They are powered by a constant current DC source. The power supply is typically 18 to 30 volts DC current limited via a constant current diode between 2 and 20 mA. Typical battery operated supplies offer 2 mA of constant current to extend battery life while continuous monitoring systems offer more current order to drive longer cables.



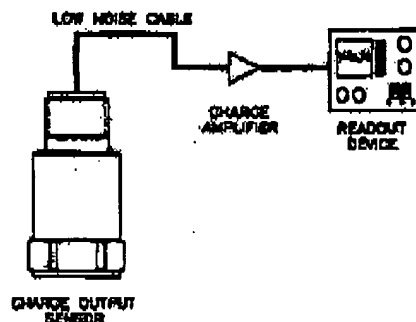
The signal output of an ICP® sensor is a low impedance voltage signal proportional to the dynamic measurement such as force, pressure, or vibration. This voltage signal is carried on a DC bias voltage. The AC dynamic signal is superimposed on the DC bias voltage and is allowed to swing between the supply voltage and ground. Unlike an operational amplifier (Op Amp) that requires a plus and minus supply and allows the signal to "ride" on ground "swing" between the plus and minus "rails," the ICP® requires the output signal to be DC biased.

IMI Technical Information

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This DC bias voltage is an excellent diagnostic tool. voltage provides a means of verifying that the amplifier "turned on." Typical input/output power supplies will this DC bias voltage at the output via a blocking capacitor to AC couple the signal to readout devices. By "testing" off the input into a DC volt meter, the bias voltage can be measured. While measuring the supply voltage bias voltage can be measured after the sensor is plugged in. If the meter stays at supply, something in the system open or not connected. If the meter reads "0," some the system is shorted. If the meter reads approximately half the supply voltage, then the sensor and cabling functioning properly.

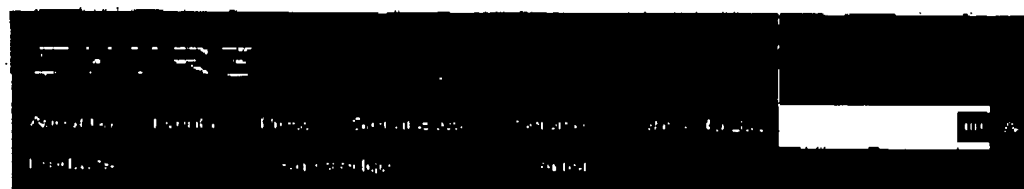

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Educational Materials

Attachment 2

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Knowledge &gt; KBase &gt; Educational Materials &gt; Phantom Power and Bias Voltage

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## phantom power and bias voltage: is there a difference?

Many users of professional audio equipment believe there is no difference between phantom power and bias voltage. Not true! Phantom and bias are not interchangeable. This page explains the differences between phantom and bias, and addresses common misconceptions.

**Phantom power** is a dc voltage (11 - 48 volts) which powers the preamplifier of a condenser microphone. Phantom power is normally supplied by the microphone mixer; may also be supplied by a separate phantom power supply. Phantom requires a baler circuit in which XLR pins 2 and 3 carry the same dc voltage relative to pin 1. So if a mic supplies 48 volts of phantom, XLR pins 2 and 3 of the microphone cable each carry 41 dc relative to pin 1. Of course, the mic cable carries the audio signal as well as the phantom voltage.

Mixers that supply phantom power contain current-limiting resistors which act as control valves. If the microphone or cable is improperly wired, these resistors limit the flow of current to the microphone and thereby prevent damage to the phantom supply circuit.

A balanced dynamic microphone is not affected by phantom power. However, an unbalanced dynamic microphone will be affected. Although the microphone will probably not be damaged, it will not work properly.

**Bias** is a dc voltage (1.5 - 9 volts, typically) that is provided on a single conductor.

Unlike phantom power, bias does not require a balanced circuit. Bias supplies power to a Junction Field Effect Transistor (JFET) connected to the output of an electret condenser element. The JFET acts as an impedance converter which is a necessity in any microp design that uses a condenser element. A condenser element has a high output impedance (>1,000,000 ohms). The JFET input loads the output of the condenser element with a higher impedance (>10,000,000 ohms) to minimize loss of signal level. Also, the JFET output provides a low source impedance (<1,000 ohms) to feed the microphone preamplifier.

In some condenser microphones, the bias voltage must be supplied on the same conductor as the audio. Condenser elements with a built-in JFET use this configuration and employ a single conductor, shielded cable. Other condenser microphones utilize separate conductors for bias and for audio. Consult the manufacturer's data sheet to find out the exact wiring configuration.

A dynamic microphone should not be connected to an input that supplies bias voltage (as a wireless transmitter) because the audio and the bias voltage will travel down the conductor. If this occurs, the frequency response of the microphone may be altered or the audio signal distorted. If a dynamic microphone must be connected to an input with

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Attachment 2

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voltage, a blocking capacitor must be used. The blocking capacitor is placed in series with the hot conductor of the microphone. The capacitor passes the audio that is present on the hot conductor while blocking the dc bias voltage. The capacitor must have enough capacitance to pass the audio signal without degradation. The exact value depends on the electronic characteristics of the microphone circuit and must be calculated for each microphone.

Remember, in a typical electret condenser microphone, it is the JFET that requires unbalanced bias and the preamplifier that requires balanced phantom power. Therefore, condenser microphones that require phantom power will not work with an input that supplies bias, e.g., a wireless transmitter.

Once again, phantom and bias are not interchangeable!

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